REMARKS

This amendment responds to the Office Action of December 31, 2003.

The status of the claims is as follows:

Claims 1, 8-11, 18-21, 24 and 25 are amended. No claims are cancelled and no claims are added.

Drawings

As a preliminary matter, and as stated above, formal drawings are submitted herewith in response to the drawing objection.

Claim rejections - 35 USC §103

Claims 1-26 were presented for examination. Of these, claims 1-7, 11-17 and 21-23 were rejected under §103(a) as unpatentable over Applicant's admitted prior art in view of Lewis '190. Reconsideration is requested.

To briefly reiterate from the specification, the present invention relates to a method, apparatus and interface for communicating between a controller and a device, in particular a Digital-to-Analog Converter (DAC), with double buffered inputs. This is achieved by providing a data transfer control signal **and** a data transfer delay signal wherein in a first logic state the data transfer signal prevents transfer of input data from one or more input registers into said one or more latchable registers in the DAC until after a transition to a second logic state occurs on the data transfer delay signal. This design approach provides maximum control and flexibility to improve the data conversion in the DAC that permits register updates to progress as quickly as possible without interfering with ongoing data conversions.

The Office Action rejects claim 1 as obvious over the prior art described and acknowledged in the introduction of the present application and Lewis (U.S. Patent No. 5,347,190). In response, claim 1 has been amended to include a Digital-to-Analog Converter (DAC) to replace the term "device" in order to clarify what the claim is covering. As noted, on page 2 lines 10 to 21 of the description, double buffered DACs enable rapid updating of input registers combined with simultaneous data transfer for all DACs within a device. Unfortunately,

a problem with these devices is that there is no way of determining precisely how these input registers can be updated rapidly, since there is no indication as to whether the internal conversion operation of a particular DAC has been completed, in order to maximise the speed of the data conversion.

In accordance with exemplary embodiments of the present invention this problem, as well as other drawbacks and limitations of conventional data conversion in DACs, is overcome by having a data transfer control signal and a data transfer delay signal to allow high speed data conversion in the DAC to take place at maximum efficiency.

Starting from the acknowledged prior art, the Examiner contends that it would be obvious to combine the acknowledged prior art with Lewis to arrive at the invention of original claim 1. The Applicant respectfully disagrees with this assertion, and offers amended claim 1 to moot the rejection.

Lewis, which discloses a rather complex and convoluted system, teaches a self-contained data conversion system for use in a magnetic bearing system. The summary of the invention at columns 2-3 cites a magnetic bearing system in all of its advantages (and claims) and is focussed on data conversion in a magnetic bearing system. Additionally the US references cited by Lewis also indicate the focus of this US patent to be substantially different from that of the present invention. Lewis only operates for Analog to Digital applications and **not** in a DAC-specific application. While the word "device" in original claim 1 might inadvertently been so broad as to encompass an ADC, the explicit reference to a DAC in amended claim 1 establishes the irrelevancy of the Lewis ADC technology. As taught in Column 23, lines 31 et seq, and Figure 16, Lewis implements digital dynamic correction based on Analog to Digital Converter (ADC) feedback from the analog start (and end) point of the signal chain, catching DAC inaccuracies and all subsequent contributors in the signal chain. This is an example of analog system calibration using digital means obtained from an Analog to Digital conversion.

The present invention, by contrast, is at least partly directed to pre-calculating the converter and subsequent (DAC) or preceding (ADC) signal chain transfer function correction, which is a complete Transfer function approach and not application limited as in Lewis. Lewis relies on a control loop with both ADCs and DACs, but with ADCs closing the loop, setting the accuracy limitations. The present invention operates by using a calibration technique which

utilises a pre-calculated transfer function correction such that there is **only** digital operation in the data path.

Consequently it would not have been obvious to one of ordinary skill to combine the acknowledged prior art with Lewis to arrive at the invention of present claim 1 (or any other independent claim). Even if an ordinary skilled person in the art had attempted to combine the acknowledged prior art with Lewis, that person would have had to incorporate many analog/mixed-signal components of Lewis into any solution and still would not have arrived at the invention of present claim 1 (or any other independent claim). Additionally the incorporation of any analog/mixed-signal components of Lewis into any solution is highly undesirable in high speed DAC systems as it will slow down the data conversion of the DAC. See introduction page 3, lines 17 to 21.

Therefore, amended claim 1 defines an invention which is neither anticipated nor rendered obvious by the prior art.

Independent claims 11 and 21 recite an apparatus and a communications interface, respectively, with similar features to those discussed above with regard to claim 1. Accordingly, claims 11 and 21 are patently distinguishable over the prior art for at least those reasons stated above with regard to claim1.

Claims 2-6, 12 –17 and 21- 23 variously depend on claims 1, 11 and 21, and are therefore, patently distinguishable over the prior art for at least those reasons stated above.

Allowable Subject Matter

Applicant notes with appreciation the indication that claims 8-10, 18-20 and 24-25 are only "objected to" as depending upon a rejected base claim. In view of the above amendment and discussion of the base independent claims, however, Applicant believes it is premature to consider rewriting any of the "objected to" claims independently.

The allowance of claim 26 is also noted with appreciation.

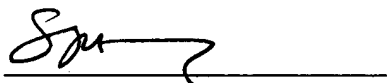
The Examiner has stated, with respect to all of the claims that are either allowed or allowable if rewritten, that allowability resides in the prior art not specifically teaching using an open drain data transfer delay signal/device between the conversion device and the controller in a wired-Or configuration as claimed. Applicant notes that this statement causes confusion in the

record and Applicant does not agree with it. For example, the reference to a "wired-Or configuration" can only apply to claim 26. Applicant therefore suggests that paragraph 7 on page 4 of the Office Action is intended to apply only to claim 26. Nevertheless, Applicant still objects that the Examiner has indicated that allowability resides in the prior art not teaching one specific aspect of the claimed method. While it may or may not be true that claim 26 is novel in light of the fact that the prior art does not show "providing open-drain, bi-directional data transfer delay signals in a wired-Or configuration from the data conversion devices to the controller", the claimed subject matter is a method comprising two additional steps and still further limitations that are not covered in the Examiner's remarks. However, the statute and case law inform us that it is the claim as a whole that does (or does not) merit patentability and allowance. Applicant objects to any suggestion that patentability resides as *only* in the feature identified by the Examiner. The cited references fail to provide a teaching of much more than the short clause extracted by the Examiner for exemplification.

Conclusion

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully Submitted,



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